

What Is Claimed Is:

1 1. An electrostatic discharge protection device is located
2 between a pad and an internal circuit, and is coupled to a first
3 level signal and a second level signal, comprising:

4 a device for detecting the voltage level of the first level
5 signal, wherein when the voltage level of the first level signal
6 reaches a first predetermined value, the voltage detecting
7 device outputs a detecting result signal;

8 a signal converting device for outputting the second level
9 signal when the detected result signal is recieved;

10 a first switch coupled to a connection point between the pad
11 and the internal circuit, wherein the first switch has a first
12 controlling gate and turns on when the voltage level of the pad
13 reaches a second predetermined voltage level;

14 a second switch coupled to the connection point between the
15 pad and the internal circuit, wherein the second switch has a
16 second controlling gate and turns on and raises the voltage value
17 of the first level signal when the voltage level of the pad
18 reaches a third predetermined voltage level; and

19 a third switch coupled to the connection point between the
20 pad and the internal circuit, wherein the third switch has a
21 third controlling gate and turns on when the voltage level of
22 the pad reaches the second predetermined voltage level and the
23 third controlling gate receives the second level signal.

1 2. The electrostatic discharge protection device as claimed
2 in claim 1, wherein the first switch and the third switch are
3 NMOS transistors.

1 3. The electrostatic discharge protection device as claimed
2 in claim 2, wherein the second switch is a PMOS transistor.

1 4. The electrostatic discharge protection device as claimed
2 in claim 3, wherein the voltage detecting device comprises at
3 least one serial diode, and turn-on voltage of the serial diodes
4 is between the first level signal and the first predetermined
5 voltage level.

1 5. The electrostatic discharge protection device as claimed
2 in claim 4, wherein the signal converting device comprises:
3 a switching circuit coupled to the voltage detecting device,
4 wherein the switching circuit outputs a ground level enable
5 signal when receiving the detecting result signal; and
6 a driving circuit coupled to the switching circuit, the
7 driving circuit outputs the second level signal when receiving
8 the ground level enable signal.

1 6. The electrostatic discharge protection device as claimed
2 in claim 5, wherein the first level signal is a power source
3 signal.

1 7. The electrostatic discharge protection device as claimed
2 in claim 6, wherein the second level signal is ground level.

1 8. The electrostatic discharge protection device as claimed
2 in claim 7, wherein the second predetermined voltage level is
3 a break down voltage of the NMOS transistor.

1 9. The electrostatic discharge protection device as claimed
2 in claim 8, wherein the third predetermined voltage level is a

3 voltage difference to make the PMOS transistor generate leakage
4 current.

1 10. The electrostatic discharge protection device as
2 claimed in claim 5, wherein the first controlling gate, the
3 second controlling gate, and the third controlling gate are
4 gates of a MOS transistor.

1 11. An electrostatic discharge protection device located
2 between a pad and an internal circuit, and is coupled to a first
3 level signal, a second level signal, and a third level signal,
4 comprising:

5 a voltage detecting device for detecting the voltage level
6 of the third level signal, wherein when the voltage level of the
7 third level signal reaches a first predetermined value, the
8 voltage detecting device outputs a detecting result signal;

9 a switching circuit coupled to the voltage detecting device,
10 the switching circuit outputs a ground level enable signal when
11 receiving the detecting result signal;

12 a driving circuit coupled to the switching circuit and the
13 voltage detecting device for generating the third level signal,
14 wherein the driving circuit outputs the second level signal when
15 receiving the ground level enable signal;

16 a first switch coupled to a connection point between the pad
17 and the internal circuit, wherein the first switch has a first
18 controlling gate and turns on when the voltage level of the pad
19 reaches a second predetermined voltage level;

20 a second switch coupled to the connection point between the
21 pad and the internal circuit, wherein the second switch has a

22 second controlling gate and turns on and raises the voltage value
23 of the first level signal when the voltage level of the pad
24 reaches a third predetermined voltage level; and

25 a third switch coupled to the connection point between the
26 pad and the internal circuit, wherein the third switch has a
27 third controlling gate and turns on when the voltage level of
28 the pad reaches the second predetermined voltage level and the
29 third controlling gate receives the second level signal.

1 12. The electrostatic discharge protection device as
2 claimed in claim 11, wherein the first switch and the third
3 switch are NMOS transistors.

1 13. The electrostatic discharge protection device as
2 claimed in claim 12, wherein the second switch is a PMOS
3 transistor.

1 14. The electrostatic discharge protection device as
2 claimed in claim 13, wherein the voltage detecting device
3 comprises at least one serial diode, and turn-on voltage of the
4 serial diodes is between the third level signal and the first
5 predetermined voltage level.

1 15. The electrostatic discharge protection device as
2 claimed in claim 14, wherein the first level signal is power
3 source signal.

1 16. The electrostatic discharge protection device as
2 claimed in claim 15, wherein the second level signal is in ground
3 level.

1 17. The electrostatic discharge protection device as
2 claimed in claim 16, wherein the second predetermined voltage
3 level is a break down voltage of the NMOS transistor.

1 18. The electrostatic discharge protection device as
2 claimed in claim 17, wherein the third predetermined voltage
3 level is a voltage difference to make the PMOS transistor
4 generate leakage current.

1 19. The electrostatic discharge protection device as
2 claimed in claim 18, wherein the first controlling gate, the
3 second controlling gate, and the third controlling gate are
4 gates of a MOS transistor.